

# LH51256L

CMOS 256K (32K × 8) Static RAM

## FEATURES

- 32,768 × 8 bit organization
- Access times: 100/120 ns (MAX.)
- Power consumption:
  - Operating: 248 mW (MAX.)  
(T<sub>A</sub> = -40 to 85°C, minimum cycle)
  - Standby: 5.5 μW (MAX.)  
(T<sub>A</sub> = 0 to 60°C)
- Fully-static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  - 28-pin, 600-mil DIP
  - 28-pin, 450-mil SOP

## DESCRIPTION

The LH51256L is a 256K bit static RAM organized as 32,768 × 8 bits which provides low-power standby mode. It is fabricated using silicon-gate CMOS process technology.

## PIN CONNECTIONS

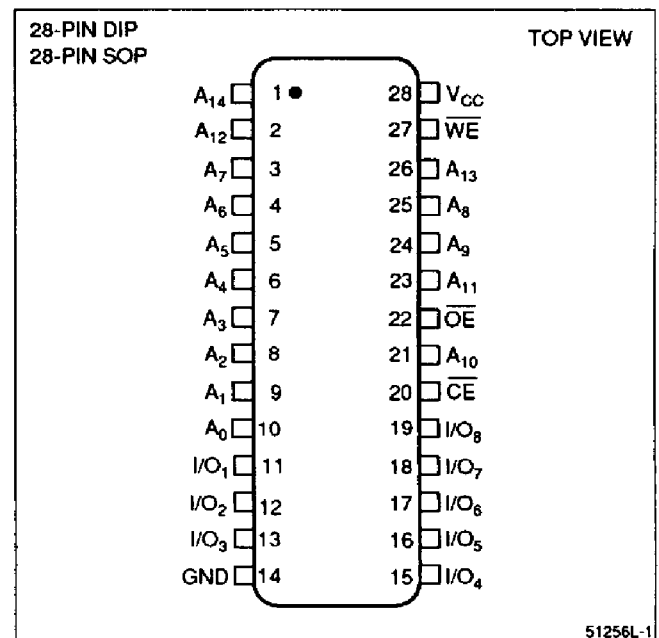


Figure 1. Pin Connections for DIP and SOP Packages

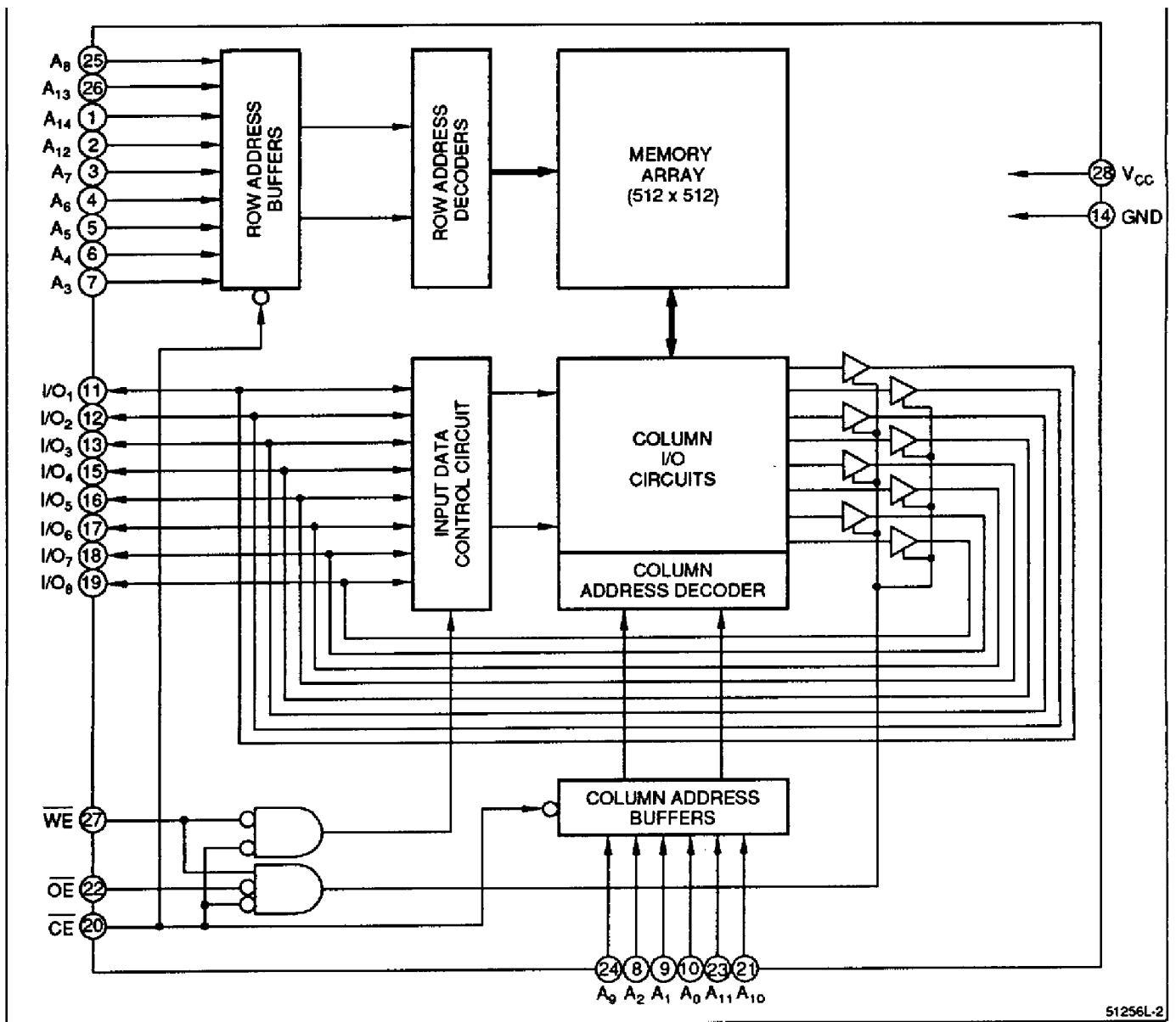


Figure 2. LH51256L Block Diagram

## PIN DESCRIPTION

SIGNAL	PIN NAME
A <sub>0</sub> - A <sub>14</sub>	Address input
$\overline{CE}$	Chip Enable input
$\overline{WE}$	Write Enable input
$\overline{OE}$	Output Enable input

SIGNAL	PIN NAME
I/O <sub>1</sub> - I/O <sub>8</sub>	Data Input/Output
V <sub>CC</sub>	Power supply
GND	Ground

## TRUTH TABLE

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	MODE	I/O <sub>1</sub> - I/O <sub>8</sub>	SUPPLY CURRENT	NOTE
H	X	X	Non selected	High-Z	Standby (I <sub>SB</sub> )	1
L	L	X	Write	D <sub>IN</sub>	Operating (I <sub>CC</sub> )	1
L	H	L	Read	D <sub>OUT</sub>	Operating (I <sub>CC</sub> )	
L	H	H	Output disable	High-Z	Operating (I <sub>CC</sub> )	

### NOTE:

1. X = H or L

## ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V <sub>CC</sub>	-0.3 to +7.0	V	1
Input voltage	V <sub>IN</sub>	-0.3 to +7.0	V	1
Operating temperature	T <sub>opr</sub>	-40 to +85	°C	
Storage temperature	T <sub>stg</sub>	-55 to +150	°C	

### NOTE:

1. The maximum applicable voltage on any pin with respect to GND.

## RECOMMENDED OPERATING CONDITIONS (T<sub>A</sub> = -40 to +85°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V <sub>CC</sub>	4.5	5.0	5.5	V
Input voltage	V <sub>IH</sub>	2.2		V <sub>CC</sub> + 0.3	V
	V <sub>IL</sub>	-0.3		0.8	V

## DC CHARACTERISTICS (V<sub>CC</sub> = 5 V ± 10%, T<sub>A</sub> = -40 to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input leakage current	I <sub>LI</sub>	V <sub>CC</sub> = 5.5 V V <sub>IN</sub> = 0 to V <sub>CC</sub>			1	μA
Output leakage current	I <sub>LO</sub>	$\overline{CE}$ or $\overline{OE}$ = V <sub>IH</sub> , V <sub>IO</sub> = 0 to V <sub>CC</sub>			1	μA
Operating current	I <sub>CC</sub>	$\overline{CE}$ = V <sub>IL</sub> , Outputs open			45	mA
Standby current	I <sub>SB1</sub>	$\overline{CE}$ = V <sub>IH</sub>			10	mA
	I <sub>SB</sub>	$\overline{CE} \geq V_{CC} - 0.2$ V T <sub>A</sub> = 0 to +60°C			1	μA
		$\overline{CE} \geq V_{CC} - 0.2$ V T <sub>A</sub> = -40 to +85°C				5
Output voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2.1 mA			0.4	V
	V <sub>OH</sub>	I <sub>OH</sub> = -1.0 mA	2.4			V

## AC CHARACTERISTICS

### (1) READ CYCLE (V<sub>CC</sub> = 5 V ± 10%, T<sub>A</sub> = -40 to +85°C)

PARAMETER	SYMBOL	LH51256/N-10L		LH51256/N-12L		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
Read cycle time	t <sub>RC</sub>	100		120		ns	
Address access time	t <sub>AA</sub>		100		120	ns	
Chip enable access time	t <sub>ACE</sub>		100		120	ns	
Output enable access time	t <sub>OE</sub>		50		60	ns	
Output hold time	t <sub>OH</sub>	5		5		ns	
$\overline{CE}$ Low to output in Low-Z	t <sub>LZ</sub>	5		5		ns	1
$\overline{OE}$ Low to output in Low-Z	t <sub>OLZ</sub>	5		5		ns	1
$\overline{CE}$ High to output in High-Z	t <sub>HZ</sub>	0	30	0	30	ns	1
$\overline{OE}$ High to output in High-Z	t <sub>OHZ</sub>	0	30	0	30	ns	1

## (2) WRITE CYCLE ( $V_{CC} = 5 V \pm 10\%$ , $T_A = -40$ to $+85^\circ\text{C}$ )

PARAMETER	SYMBOL	LH51256/N-10L		LH51256/N-12L		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
Write cycle time	t <sub>wc</sub>	100		120		ns	
$\overline{\text{CE}}$ Low to end of write	t <sub>cw</sub>	90		100		ns	
Address valid to end of write	t <sub>aw</sub>	90		100		ns	
Address setup time	t <sub>as</sub>	5		5		ns	
Write recovery time	t <sub>wr</sub>	15		15		ns	
Write pulse width	t <sub>wp</sub>	50		50		ns	
Input data setup time	t <sub>ow</sub>	30		30		ns	
Input data hold time	t <sub>dh</sub>	10		10		ns	
$\overline{\text{WE}}$ High to output in High-Z	t <sub>ow</sub>	0		0		ns	1
$\overline{\text{WE}}$ Low to output in High-Z	t <sub>wz</sub>	0	30	0	30	ns	1
$\overline{\text{OE}}$ High to output in High-Z	t <sub>ohz</sub>	0	30	0	30	ns	1

### NOTE:

- Active output to high-impedance and high-impedance to output active tests specified for a  $\pm 500$  mV transition from steady state levels into the test load.  $C_{\text{LOAD}} = 5$  pF.

## AC TEST CONDITIONS

PARAMETER	MODE
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Timing reference level	1.5 V
Output load conditions	1TTL + $C_L = 100$ pF (Includes scope and jig capacitance)

## CAPACITANCE <sup>1</sup> ( $T_A = 25^\circ\text{C}$ , $f = 1\text{MHz}$ )

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 0 V			7	pF
Input/output capacitance	C <sub>IO</sub>	V <sub>IO</sub> = 0 V			10	pF

### NOTE:

- This parameter is sampled and not production tested.

## DATA RETENTION CHARACTERISTICS ( $T_A = -40$ TO $+85^\circ\text{C}$ )

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Data retention voltage	V <sub>CCDR</sub>	$\overline{\text{CE}} \geq V_{\text{CCDR}} - 0.2$ V	2.0			V	
Data retention current	I <sub>CCDR</sub>	V <sub>CCDR</sub> = 3.0 V, $\overline{\text{CE}} \geq V_{\text{CCDR}} - 0.2$ V, $T_A = 0$ to $+60^\circ\text{C}$ , V <sub>IN</sub> = 0 to V <sub>CCDR</sub>			0.6	μA	
		V <sub>CCDR</sub> = 3.0 V $\overline{\text{CE}} \geq V_{\text{CCDR}} - 0.2$ V, $T_A = -40$ to $+85^\circ\text{C}$ , V <sub>IN</sub> = 0 to V <sub>CCDR</sub>			3.0	μA	
$\overline{\text{CE}}$ setup time	t <sub>CDR</sub>		0			ns	
$\overline{\text{CE}}$ hold time	t <sub>RDR</sub>		t <sub>RC</sub>			ns	1

### NOTE:

- t<sub>RC</sub> = Read cycle time

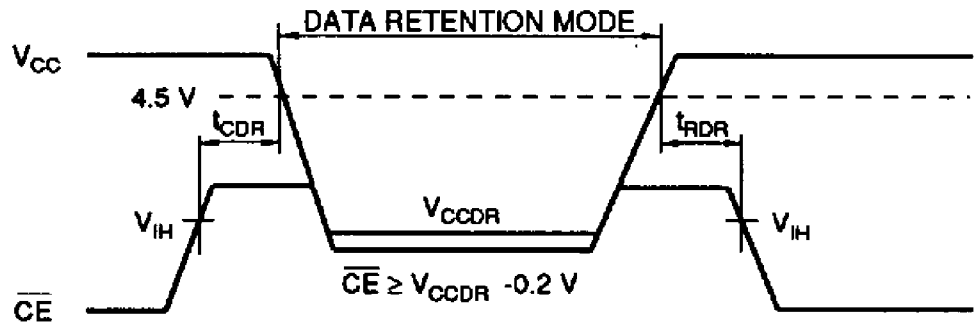
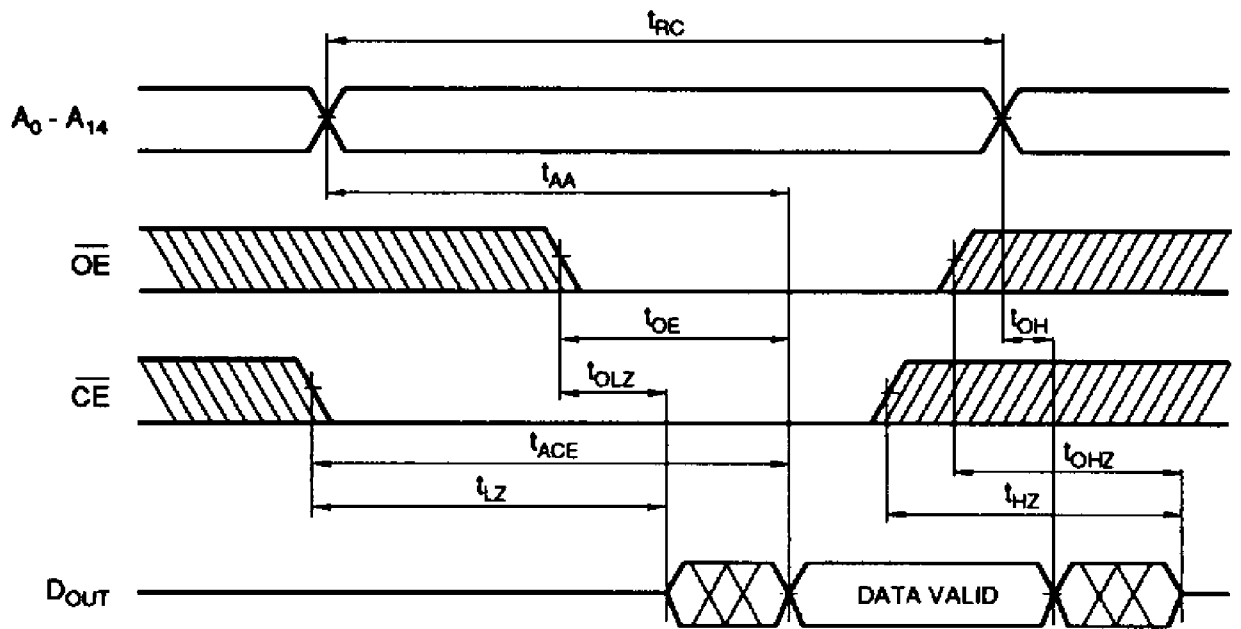
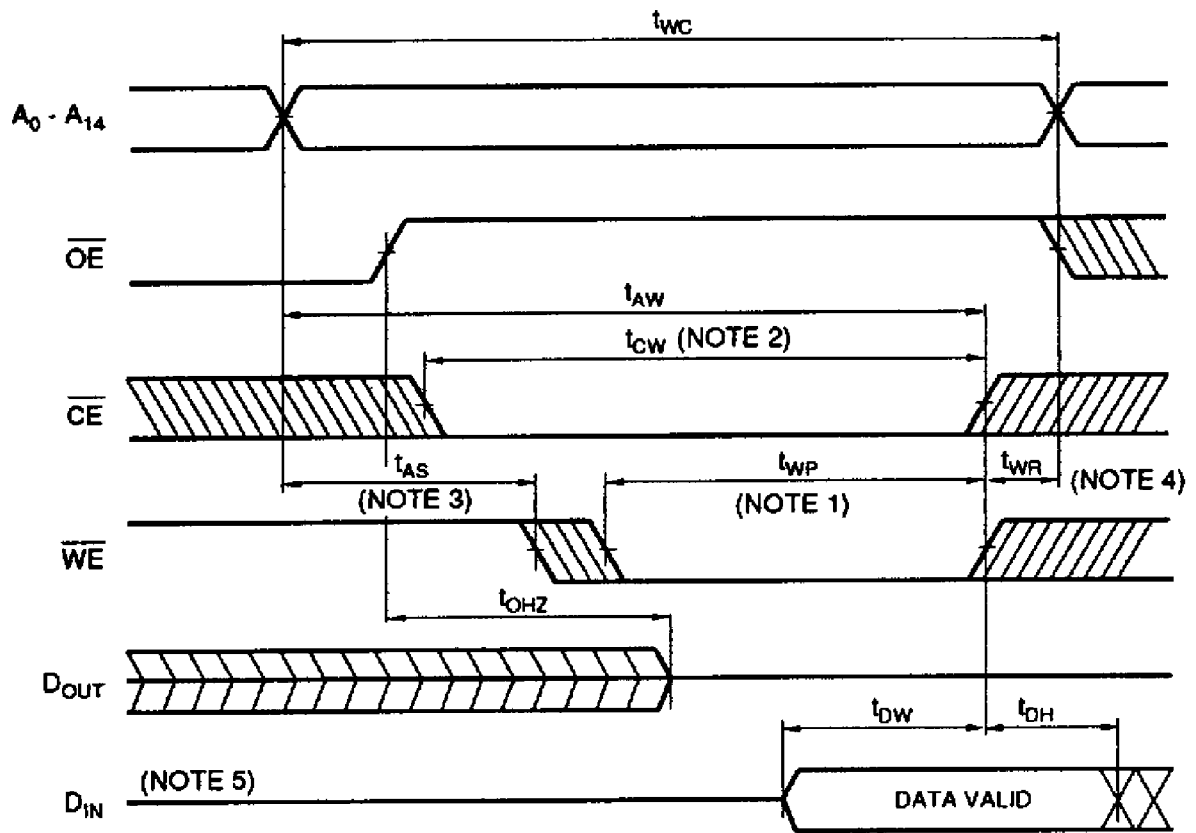


Figure 3. Data Retention Characteristics

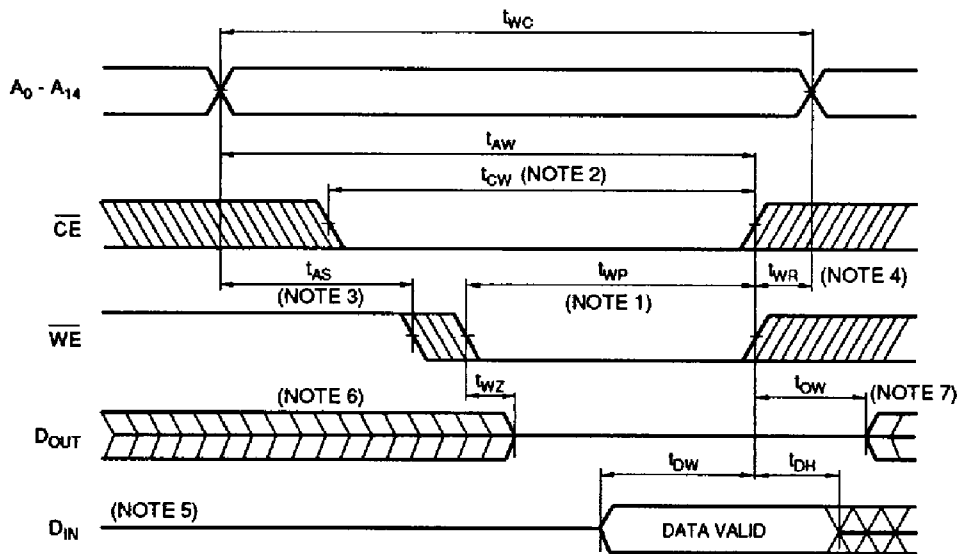


NOTE:  $\overline{WE}$  = "HIGH"



**NOTES:**

1. The write pulse occurs during the overlap ( $t_{WP}$ ) of  $\overline{CE} = \text{LOW}$  and  $\overline{WE} = \text{LOW}$ .
2.  $t_{CW}$  is defined as the time from  $\overline{CE}$  LOW transition to the end of writing.
3.  $t_{AS}$  is defined as the time from address change to the start of writing.
4.  $t_{WR}$  is defined as the time from the end of writing to the address change.
5. When the I/O pins are in the output state, input signals with the opposite logic level must not be applied.



**NOTES:**

1. The write pulse occurs during the overlap ( $t_{WP}$ ) of  $\overline{CE} = \text{LOW}$  and  $\overline{WE} = \text{LOW}$ .
2.  $t_{CW}$  is defined as the time from CE LOW transition to the end of writing.
3.  $t_{AS}$  is defined as the time from address change to the start of writing.
4.  $t_{WR}$  is defined as the time from the end of writing to the address change.
5. When the I/O pins are in the output state, input signals with the opposite logic level must not be applied.
6. If CE LOW transition occurs at the same time or after WE LOW transition, the output will remain high-impedance.
7. If CE HIGH transition occurs at the same time or prior to the WE HIGH transition, the output will remain high-impedance.

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**Figure 6. Write Cycle 2 ( $\overline{OE}$  Low)**

**ORDERING INFORMATION**

LH51256	X	- ##	
Device Type	Package	Speed	
			{ 10L 100 12L 120 Access Time (ns)
			{ Blank 28-pin, 600-mil DIP (DIP28-P-600) N 28-pin, 450-mil SOP (SOP28-P-450)
			CMOS 256K (32K x 8) Static RAM, Low-power standby

**Example:** LH51256N-10L (CMOS 256K (32K x 8) Static RAM, 100 ns, 28-pin, 450-mil SOP)

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